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(71) Applicant: LAM RESEARCH CORPORATION [US/US]; P0487.PCT, 4650 Cushing Parkway, Fremont, CA 94538-6516 (US).

(72) Inventors: MOREY, Ian, J.; 630 North San Pedro Street #5B, San Jose, CA 95110 (US). ELLINGBOE, Susan; 43100 Paseo Padre Parkway, Fremont, CA 94539 (US). FLANNER, Janet, M.; 4942 Rocklin Drive, Union City, CA 94587 (US). JANOWIAK, Christine, M.; 38455 Bronson Street #126, Fremont, CA 94536 (US). LANG, John; 1559 Dennis Avenue, Milpitas, CA 95035 (US).

(74) Agent: LEE, Michael; Beyer Weaver & Thomas, LLP, Post Office Box 130, Mountain View, CA 94042-0130 (US).

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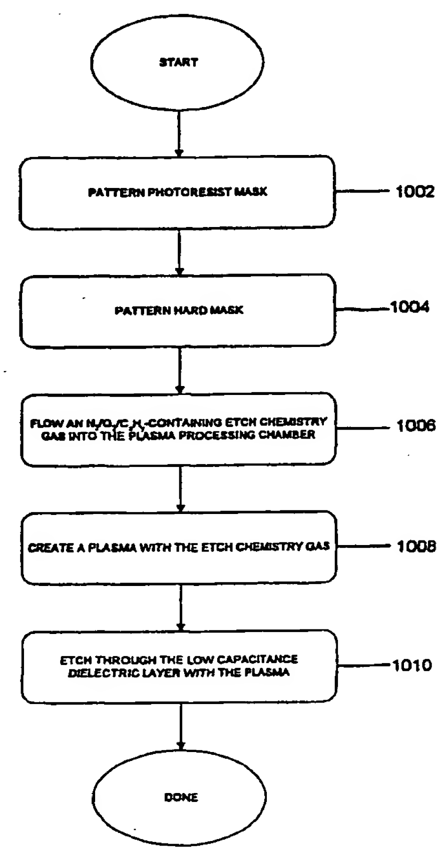
(57) Abstract

Techniques for etching through a low capacitance dielectric layer in a plasma processing chamber are disclosed. The techniques use an etch chemistry that includes N_2, O_2, and a hydrocarbon. By etching the low capacitance dielectric layer with a plasma created out of the etch chemistry, fast etch rates can be obtained while also maintaining profile control and preserving critical dimension of the resultant opening (e.g., via/trench) being etched in the low capacitance layer.



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TECHNIQUES FOR ETCHING A LOW CAPACITANCE DIELECTRIC LAYER

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation-in-part of U.S. Application No. 09/135,419, entitled "TECHNIQUES FOR ETCHING A LOW CAPACITANCE DIELECTRIC LAYER ON A SUBSTRATE", and filed on August 17, 1998, the disclosure of which is incorporated herein by reference for all purposes. This application also claims the benefit of U.S. Provisional Application No. 60/132,645, entitled "TECHNIQUES FOR ETCHING A LOW CAPACITANCE DIELECTRIC LAYER", and filed on May 5, 1999, the disclosure of which is incorporated herein by reference for all purposes.

BACKGROUND OF THE INVENTION

The present invention relates to the fabrication of semiconductor integrated circuits (IC's). More particularly, the present invention relates to improved techniques for etching through an IC layer stack, including a low capacitance dielectric layer, during IC fabrication.

In the manufacturing of certain semiconductor integrated circuits, a low dielectric constant (low-K) material may sometimes be employed as the material in a dielectric layer in order to reduce the capacitance of devices that are formed and to improve their electrical performance. As in all dielectric layers, there is typically a need to etch vias or trenches through the dielectric layer in order to form metal interconnects therethrough. The process of forming a via/trench through the low capacitance dielectric layer is described below.

To facilitate discussion, Fig. 1 illustrates a representative layer stack 100, including a photoresist layer 102, a hard mask layer 104, a low capacitance dielectric layer 106, and an etch stop layer 108. Etch stop layer 108 may represent, for example, an etch stop layer for a dual damascene process and is typically formed of a suitable etch stop material such as TiN, SiN, TEOS, or the like. Low capacitance dielectric layer 106 represents a layer of organic low-K material such as SILK by Dow Chemical, Flare by Allied Signal, BCB by Dow Chemical, Parylene by Novellus, or the like. The etch chemistry may also etch non-low-K materials such as organic films like photoresist.

Above low capacitance dielectric layer 106, there is shown disposed a hard mask layer 104, which is typically formed of a material such as SiN, SiON (silicon oxynitride) or TEOS. Hard mask layer 104 represents the masking layer that is employed to etch the via/trench in low capacitance dielectric layer 106. The hard mask layer is employed since photoresist is typically ineffective as a masking material when etching the organic low-K material of low capacitance dielectric layer 106. This is because the photoresist material and the organic low-K material tend to have similar chemical characteristics, tend to require a similar etch chemistry, and/or tend to have a similar etch rate. To pattern the hard mask out of hard mask layer 104, photoresist layer 102 is provided. Photoresist layer 102 may represent, for example, a layer of deep UV or conventional photoresist material.

In Fig. 2, photoresist layer 102 is patterned using a conventional photoresist patterning process. The patterning of photoresist layer 102 creates an opening 202 through which hard mask layer 104 may be etched in a subsequent hard mask etch process.

In Fig. 3, a hard mask etch process is employed to extend opening 202 through hard mask layer 104. In one example, hard mask layer 104 represents a TEOS layer, and the hard mask etch process may take place in a plasma processing reactor using a suitable TEOS etch chemistry such as $Ar/C_4F_8/C_2F_6/O_2$ or a conventional TEOS etchant.

In Fig. 4, the low capacitance dielectric layer 106 is being etched. The etching of low capacitance dielectric layer 106 typically takes place in a plasma processing reactor. Low capacitance dielectric layer 106 is typically etched using an oxygen-containing gas (such as O_2, CO, CO_2, or the like). A diluent such as N_2 is typically added to the etchant gas employed to etch through the low capacitance dielectric material. For reasons which shall be explained shortly hereinafter, a passivating agent such as a fluorocarbon gas is also typically added to the etch chemistry.

As is well known, the oxygen species employed to etch through low capacitance dielectric layer 106 tends to etch isotropically, causing the sidewalls in opening 202 to bow instead of maintaining the desired vertical sidewall profile. Fig. 5 illustrates the bowing sidewall that occurs when the etch is allowed to proceed isotropically through low capacitance dielectric layer 106. The bowing effect is exacerbated if over-etching is required to compensate for etch nonuniformity across the wafer. This bowing effect degrades profile control, for example, causing the formation of re-entrant profiles, which are profiles that have

angles greater than 90 degrees, and cause difficulties in subsequent processing steps such as metal fill.

To maintain profile control and prevent the aforementioned sidewall bowing problem, in addition to the oxygen-containing gas, the prior art typically employs a fluorocarbon such as C_4F_8, C_2HF_5, CH_2F_2, or the like as a passivating agent. However, while the addition of the fluorocarbon passivating agent helps preserve the vertical sidewall profile, it tends to facet first the photoresist and subsequently the hard mask, which in turn enlarges opening 202 as the etch proceeds through low capacitance dielectric layer 106.

To elaborate, the oxygen species that is employed to etch through the low capacitance dielectric layer 106 also attacks the overlying photoresist material in photoresist layer 102. Consequently, the thickness of photoresist layer 102 is reduced as the etch proceeds through low capacitance dielectric layer 106. Because the oxygen species attacks the photoresist material isotropically, the photoresist mask often pulls back in regions 402 and 404 of the via/trench. As the photoresist material is worn away by the oxygen species and the photoresist material is pulled back in regions 402 and 404 as shown in Fig. 4, the TEOS hard mask material of hard mask layer 104 is exposed to the fluorocarbon etchant that is added for passivation purposes. Since fluorocarbon is an etchant of TEOS, the exposed hard mask material in regions 408 and 410 are also etched away as time goes on, causing the opening in hard mask layer 104 to enlarge. The enlargement of the opening in hard mask layer 104 in turn enlarges the via/trench to be etched through low capacitance dielectric layer 106. With this enlargement, the critical dimension of the via/trench are lost or destroyed. The result is shown in Fig. 6 wherein the resultant via/trench has a larger cross-section than intended, where width (w) indicates the intended cross-section.

The use of a fluorocarbon additive also narrows the process window of the low capacitance dielectric layer etch. If too much fluorocarbon is added to the etch chemistry, the etch rate of the low capacitance dielectric layer will be reduced dramatically, until etch stoppage eventually occurs. If too little fluorocarbon is added, there may be insufficient passivation to maintain the desired vertical sidewall profile.

In view of the foregoing, there is a need for improved techniques for etching through a low capacitance dielectric layer while maintaining profile control, preserving critical dimension of the resultant via/trench, and maintaining a high etch rate.

SUMMARY OF THE INVENTION

The present invention relates to a method for etching through a low capacitance dielectric layer in a plasma processing chamber. The method uses an etch chemistry that includes N_2, O_2, and a hydrocarbon into the plasma processing chamber. The present invention yields not only fast etch rates but also maintains profile control and preserves critical dimension of the resultant opening (e.g., via/trench) being etched in the low capacitance layer.

In one embodiment, the present invention relates to a method for etching through a low capacitance dielectric layer in a plasma processing chamber. The low capacitance dielectric layer is disposed below a hard mask layer on a substrate. The method includes flowing an etch chemistry that includes N_2, O_2, and a hydrocarbon into the plasma processing chamber. A plasma is then created out of the etch chemistry. The method also includes etching, using the plasma, through the low capacitance dielectric layer through openings in the hard mask layer.

In accordance with another embodiment, the etch chemistry further includes a fluorocarbon-containing gas. The fluorocarbon-containing gas chemistry is, for example, effective for etching a silicon-containing low-K dielectric layer. In still another embodiment, the plasma processing chamber represents an inductive-type plasma processing chamber. In yet another embodiment, the plasma processing chamber represents a capacitive-type plasma processing chamber.

These and other features of the present invention will be described in more detail below in the detailed description of the invention and in conjunction with the following figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings, which are not drawn to scale to simplify the illustration, where like reference numerals refer to similar elements, and in which:

Fig. 1 illustrates an exemplary prior art IC layer stack.

Fig. 2 illustrates the prior art IC layer stack of Fig. 1 after the photoresist layer is patterned.

Fig. 3 illustrates the prior art IC layer stack of Fig. 1 after the hard mask layer is patterned.

Fig. 4 illustrates the beginning of the etch through the low capacitance dielectric layer and the pull back of the photoresist which occurs.

Fig. 5 illustrates the bowing that may occur in the sidewalls of the via when the prior art etch chemistry is employed to etch through the low capacitance dielectric layer.

Fig. 6 illustrates the degradation of the critical dimension of the via that may occur when the prior art etch chemistry is employed to etch through the low capacitance dielectric layer.

Fig. 7 illustrates an exemplar via of a low capacitance dielectric layer that is etched using one embodiment of the present invention.

Fig. 8 illustrates a simplified schematic of the TCP™ 9100PTX plasma reactor, representing one of the plasma reactors suitable for practicing the present invention.

Fig. 9 illustrates a simplified schematic of the 4520 XLE plasma reactor, representing one of the plasma reactors suitable for practicing the present invention.

Fig. 10 illustrates, in accordance with one embodiment of the present invention, a flowchart of the operations of the inventive low capacitance dielectric etch.

DETAILED DESCRIPTION OF THE INVENTION

The present invention will now be described in detail with reference to a few preferred embodiments thereof as illustrated in the accompanying drawings. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process steps and/or structures have not been described in detail in order to not unnecessarily obscure the present invention.

In accordance with one aspect of the present invention, a organic low capacitance dielectric material of the low capacitance dielectric layer is etched in a plasma reactor using an etch chemistry that includes hydrocarbons. In one embodiment, the etch chemistry is N_2, O_2, and C_xH_y. Optionally, a small amount of a fluorocarbon-containing gas may be included in the etch chemistry for use in certain applications such as etching silicon-containing low capacitance dielectric layers.

Several embodiments of an inventive N_2/H_2 chemistry are further described in commonly assigned U.S. Patent Application No. 09/135,419, filed August 17, 1998 entitled, "IMPROVED TECHNIQUES FOR ETCHING A LOW CAPACITANCE DIELECTRIC LAYER ON A SUBSTRATE", which is incorporated herein by reference. The N_2/H_2 chemistry does achieve the desired results of good vertical profile and critical dimension (CD) control, but etches at a low etch rate. Moreover, in using the N_2/H_2 chemistry, if over-etching is required to compensate for etch nonuniformity across the wafer, there may be a slight bowing effect in the etched opening. The inventive $N_2/O_2/C_xH_y$-containing etch chemistry provides the desired benefits of good vertical profile and critical dimension control with a high etch rate, for example, between 2000 Å/min - 8000 Å/min, preferably between 5000 Å/min - 8000 Å/min, while avoiding the undesired characteristics of bowed sidewalls, loss of critical dimension, loss of profile control, or lower etch rate, by way of example, that are present in the etch results obtained by using alternative etch chemistries.

The inventive $N_2/O_2/C_xH_y$-containing etch chemistry may be used in etching a low capacitance dielectric layer similar to the low capacitance dielectric layer that is present in the layer stack of Fig. 1. By way of example, the etching process begins much like the partial process flow shown in Figs. 1-4, with a layer stack that includes a photoresist layer, a hard mask layer, a low capacitance dielectric layer, and an etch stop layer. The photoresist layer is patterned by a conventional photoresist patterning process to create an opening, followed by a hard mask etch process to extend that opening through the hard mask layer. Then the low capacitance dielectric layer is etched using the inventive $N_2/O_2/C_xH_y$-containing etch chemistry.

The oxygen species that is employed to etch through the low capacitance dielectric layer also attacks the overlying photoresist layer. Consequently, the thickness of photoresist layer is reduced as the etch proceeds through the low capacitance dielectric layer. Because the

oxygen species attacks the photoresist material isotropically, the photoresist mask may also pull back in regions of the via/trench, and may even be completely removed when the etching reaches the etch stop layer. This may be a desired effect in some applications which call for the removal of photoresist during etching.

In the inventive $N_2/O_2/C_xH_y$-containing etch chemistry, a hydrocarbon such as C_2H_4 or CH_4 is employed as a passivating agent. The hydrocarbon component of this inventive etch chemistry, which replaces the fluorocarbon used in prior art methods, passivates the sidewalls of the etched opening, which minimizes the isotropic component of the etch through the low capacitance dielectric layer. The use of hydrocarbons eliminates the chemical component of hard mask etching, and leaves only the physical sputtering component. Although faceting of the photoresist and subsequently the hard mask still take place, in addition to the pullback of the photoresist, the absence of fluorine in the gas chemistry used for etching the low capacitance dielectric layer greatly minimizes the faceting effects. Therefore, relatively less faceting of the photoresist and the hard mask means that adequate passivation may be provided by the hydrocarbon component of the etch chemistry to maintain the desired critical dimension and vertical sidewall profile. As a result, the cross-section of the etched opening is not enlarged and critical dimension control is achieved.

Fig. 7 shows an exemplary via/trench 702 that has been etched in low capacitance dielectric layer 106 using the inventive $N_2/O_2/C_xH_y$-containing etch chemistry. Due to the passivation of the sidewalls 704 by the hydrocarbon component of the etch chemistry, a vertical profile is maintained and the desired critical dimension is achieved in spite of complete removal of the photoresist layer as well as partial erosion of hardmask 104.

It is contemplated that the inventive low capacitance dielectric material etch technique may be practiced in any suitable plasma processing reactors, including capacitive-type reactors and inductive-type low pressure, high density (e.g., $>10^9$ ions/cm^3) reactors. In a preferred embodiment, the present invention is practiced in an inductively coupled plasma processing reactor such as the TCP™ 9100PTX plasma reactor, which is available from Lam Research Corporation. Fig. 8 illustrates a simplified schematic of the TCP™ 9100PTX plasma reactor, including a plasma processing chamber 802. A dielectric window 804 is disposed below an electrode 806 and acts as the dielectric window through which the plasma within plasma processing chamber 802 may inductively couple with electrode 806. Electrode 806 represents the RF induction source and is implemented by a

coil in the example of Fig. 8. Electrode 806 is energized by a RF generator 808 via a matching network (conventional and not shown in Fig. 8 to simplify the illustration). The RF frequency of RF generator 808 may be about 13.56 MHz in one embodiment although other suitable RF frequencies may also be employed.

Within chamber 802, there may be provided a gas distribution plate 810, which preferably includes a plurality of holes for releasing gaseous source materials, e.g., the etch chemistries, into the RF-induced plasma region between gas distribution plate 810 and a wafer 812. The gaseous source materials may also be released from ports built into the walls of the chamber itself. Wafer 812 is introduced into chamber 802 and disposed on a chuck 814, which acts as a second electrode and is preferably biased by a radio frequency generator 816 (also typically via a matching network). The RF frequency of RF generator 816 may be about 4 MHz in one embodiment although other suitable RF frequencies may also be employed. Wafer 812 may be secured to chuck 814 using a conventional mechanical clamping technique or one that employs electrostatic clamping forces.

Helium cooling gas is introduced under pressure between chuck 814 and wafer 812 to act as a heat transfer medium for accurately controlling the wafer's temperature during processing to ensure uniform and repeatable etching results. During plasma etching, the pressure within chamber 802 is preferably kept low by evacuating gas through port 818, e.g., between about 1 mTorr to about 30 mTorr during the low-K dielectric etching.

In another preferred embodiment, the present invention is practiced in a capactive-type plasma processing reactor such as the 4520 XLE plasma reactor, which is available from Lam Research Corporation. Fig. 9 illustrates a simplified schematic of the 4520 XLE plasma reactor, including a plasma processing chamber 902. A gap drive 904 is disposed above a top electrode 906. Gap drive 904 is primarily used for wafer transport, though it is may sometimes be used as a process parameter. Top electrode 906 is implemented by a silicon electrode in the example of Fig. 9. Top electrode 906 is energized by a RF generator 908 via a matching network (conventional and not shown in Fig. 9 to simplify the illustration). The RF frequency of RF generator 908 may be about 27 MHz in one embodiment although other suitable RF frequencies may also be employed.

Within chamber 902, there may be provided a confinement ring 910, which preferably confines the plasma generated in the gaseous source materials, e.g., the etch chemistries, into the RF-induced plasma region between top electrode 906 and a wafer 912.

Gases enter chamber 902 through top electrode 906. The gaseous source materials may also be released from ports that may be built into the walls of the chamber itself or released around the perimeter of the electrostatic chuck 914. Wafer 912 is introduced into chamber 902 and disposed on a chuck 914, which acts as a second electrode and is preferably biased by a RF generator 916 (also typically via a matching network). The RF frequency of RF generator 916 may be about 2 MHz in one embodiment although other suitable RF frequencies may also be employed. Wafer 912 may be secured to chuck 914 using a conventional mechanical clamping technique or one that employs electrostatic clamping forces. During plasma etching, the pressure within chamber 902 is typically kept between about 10 mTorr to about 300 mTorr during the low-K dielectric etching.

Fig. 10 illustrates a flowchart of the operations of the inventive low capacitance dielectric etch process 1000 in accordance with one embodiment of the present invention. In operation 1002, a photoresist mask is patterned using a conventional photoresist patterning process. In operation 1004, a hard mask is patterned out of a hard mask layer using the earlier created photoresist mask. That is, openings in the hard mask that correspond to the openings to be formed in the low capacitance dielectric layer are etched in operation 1004. As the term is used herein, the openings in the low capacitance dielectric layer refer to features etched in the low capacitance dielectric layer and include both trenches and vias.

In operations 1006, 1008, and 1010, the low capacitance dielectric layer is etched. The etching of the low capacitance dielectric layer may take place in a separate plasma processing chamber, or more preferably, in the same plasma processing chamber that is employed for the hard mask etch. In operation 1006, an $N_2/O_2/C_xH_y$-containing etch chemistry is flowed into the plasma processing chamber. The $N_2/O_2/C_xH_y$-containing etch chemistry may optionally include a fluorocarbon, such as C_2F_6 or C_4F_8, which would be desirable in etching a low capacitance dielectric layer that contains silicon such as a benzo-cyclo-butene (BCB) material. In operation 1008, a plasma is created out of the $N_2/O_2/C_xH_y$-containing etch chemistry. In operation 1010, the plasma that is created out of the $N_2/O_2/C_xH_y$-containing etch chemistry is allowed to etch through the low capacitance dielectric material of the low capacitance dielectric layer through the openings in the hard mask. After the low capacitance dielectric layer is etched through at operation 1010, the low capacitance dielectric etch process 1000 ends. In most cases, however, an overetch

step may be employed to compensate for any etch nonuniformity across the wafer. Thereafter, conventional processing operations may be employed to form integrated circuits from the etched wafer.

In one example, the wafer to be etched represents a 200 mm wafer having thereon a layer of the low capacitance dielectric material FLARE 2.0 underlying a hard mask layer formed of TEOS. The low capacitance dielectric layer is about 7,500 angstroms thick, and the hard mask layer is about 2,000 angstroms thick. The photoresist mask represents a deep UV photoresist mask, although any type of photoresist material may be employed. The openings to be etched have a cross-section of about 0.3 microns. The low capacitance dielectric layer etch is performed in a high density, low pressure inductively coupled plasma processing reactor known as the TCP™ 9100PTX, available from Lam Research Corp. of Fremont, California. It should be readily apparent and within the skills of one skilled in the art that the parameters provided in the examples below may be scaled and/or modified as appropriate to etch a substrate having a different dimension or to conform to the requirements of a specific plasma reactor.

In the aforementioned TCP™ 9100 PTX plasma processing system, the pressure within the plasma processing chamber may be between about 1 milliTorr (mT) and about 30 mT, more preferably between about 5 mT and about 20 mT, and preferably at about 10 mT. The top electrode power may be between about 700 watts and about 2,200 watts, more preferably between about 1200 watts and about 2000 watts, and preferably at about 1,800 watts. The bottom electrode power may be between about 50 watts and about 500 watts, more preferably between about 100 watts and about 400 watts, and preferably at about 300 watts.

In the TCP™ 9100 PTX plasma processing system used in this example, the N_2 flow may be between about 25 sccm and about 150 sccm, more preferably between about 50 sccm and about 100 sccm, and preferably at about 50 sccm. The O_2 flow may be between about 5 sccm and about 75 sccm, more preferably between about 10 sccm and about 50 sccm, and preferably at about 25 sccm. The C_xH_y flow may be between about 1 sccm and about 50 sccm, more preferably between about 5 sccm and about 30 sccm, and preferably at about 15sccm. Small amounts (e.g., < 5 sccm) of a fluorocarbon-containing gas may also be added to the $N_2/O_2/$ C_xH_y-containing etch chemistry such as when etching a

silicon-containing low capacitance dielectric layer such as BCB. By way of example, C_2F_6 or C_4F_8 may be added.

The low capacitance dielectric layer etch can also be performed in a capacitive-type plasma processing reactor such as the 4520XLE, available from Lam Research Corp. of Fremont, California. In the aforementioned 4520XLE plasma processing system, the pressure within the plasma processing chamber may be between about 10 milliTorr (mT) and about 300 mT, more preferably between about 30 mT and about 200 mT, and preferably at about 100 mT. The top electrode power may be between about 0 watts and about 2,000 watts, more preferably between about 200 watts and about 800 watts, and preferably at about 500 watts. The bottom electrode power may be between about 0 watts and about 2000 watts, more preferably between about 200 watts and about 800 watts, and preferably at about 500 watts.

In the 4520XLE plasma processing system, the N_2 flow may be between about 0 sccm and about 1000 sccm, more preferably between about 50 sccm and about 600 sccm, and preferably at about 500 sccm. The O_2 flow may be between about 5 sccm and about 500 sccm, more preferably between about 5 sccm and about 50 sccm, and preferably at about 18 sccm. The C_xH_y flow may be between about 0 sccm and about 500 sccm, more preferably between about 0 sccm and about 50 sccm, and preferably at about 18 sccm. Small amounts (e.g., < 5 sccm) of a fluorocarbon-containing gas, C_2F_6 or C_4F_8, by way of example, may also be added to the $N_2/O_2/$ C_xH_y-containing etch chemistry when etching a silicon-containing low capacitance dielectric layer such as BCB.

The percentage flow of N_2 expressed as a percentage of total flow may be between about 50% and about 95%, and in an exemplar etch process, at about 93.3%. The percentage flow of O_2 expressed as a percentage of total flow may be between about 2% and about 40%, and in an exemplar etch process, at about 3.3%. The percentage flow of C_xH_y expressed as a percentage of total flow may be between about 2% and about 40%, and in an exemplar etch process, at about 3.3%. As mentioned before, additional fluorocarbon-containing gases may also be added to the $N_2/O_2/$ C_xH_y-containing etch chemistry such as when etching a silicon-containing low capacitance dielectric layer (e.g., BCB). By way of example, C_2F_6 or C_4F_8 may be added, and the percentage flow of C_xF_y expressed as a percentage of total flow may be, by way of example, about 0.05%.

It is believed that increasing the hydrocarbon content relative to the oxygen in the etch chemistry contributes more to improving profile control than merely changing the oxygen flow. The $C_xH_y:O_2$ ratio may be between about 1:99 to about 2:1, more preferably between about 2:3 and about 3:2. In one exemplary etch, advantageous etch results were observed in an etch chemistry mixture having a $C_xH_y:O_2$ ratio of about 3:2.

As can be appreciated from the foregoing, the inventive low capacitance dielectric etch that employs an $N_2/O_2/C_xH_y$-containing etch chemistry advantageously passivates the sidewalls to maintain a substantially vertical profile and to facilitate a higher degree of critical dimension control even while etching at high etch rates. The passivation of the sidewalls, which is due to the hydrocarbon component of the improved $N_2/O_2/C_xH_y$-containing etch chemistry, allows the etched opening to maintain the substantially vertical profile as well as to facilitate a higher degree of critical dimension control. The hydrocarbon addition to the inventive etch chemistry compensates for the isotropic etch qualities of the oxygen-containing component.

While this invention has been described in terms of several preferred embodiments, there are alterations, permutations, and equivalents which fall within the scope of this invention. It should also be noted that there are may alternative ways of implementing the methods and apparatuses of the present invention. It is therefore intended that the following appended claims be interpreted as including all such alterations, permutations, and equivalents as fall within the true spirit and scope of the present invention.

CLAIMS

What is claimed is:

1. A method for etching a low capacitance dielectric layer in a plasma processing chamber, said low capacitance dielectric layer being disposed below a hard mask layer on a substrate, said method comprising:

flowing an etch chemistry that includes N_2,O_2, and a hydrocarbon into said plasma processing chamber;

creating a plasma out of said etch chemistry; and

etching, using said plasma, through said low capacitance dielectric layer through openings in said hard mask layer.

2. The method of claim 1, wherein said hydrocarbon is C_2H_4.

3. The method of claim 1, wherein said hydrocarbon is CH_4.

4. The method of claim 1, wherein said hard mask layer is formed of TEOS.

5. The method of claim 1, wherein said plasma processing chamber represents a low pressure, high density plasma processing chamber.

6. The method of claim 1, wherein said plasma processing chamber represents an inductively coupled plasma processing chamber.

7. The method of claim 1, wherein said plasma processing chamber represents a capacitive-type plasma processing chamber.

8. The method of claim 1, wherein the percentage of flow of said N_2 is between about 50% and about 95% of a total flow.

9. The method of claim 8, wherein the percentage of flow of said O_2 is between about 5% and about 40% of a total flow.

10. The method of claim 9, wherein the percentage of flow of said hydrocarbon is between about 2% and about 40% of a total flow rate.

11. The method of claim 1, wherein said hydrocarbon and said O_2 are present in the etch chemistry at a ratio of between about 2:1 and about 1:99.

12. The method of claim 6, wherein said plasma processing chamber represents an inductively coupled plasma processing chamber, and

wherein said plasma processing chamber is maintained at a pressure between 1mTorr and 30 mTorr.

13. The method of claim 7, wherein said plasma processing chamber represents a capacitive-type plasma processing chamber, and

wherein said plasma processing chamber is maintained at a pressure between 10mTorr and 300 mTorr.

14. The method of claim 1, wherein said hard mask layer is disposed below a photoresist layer.

15. The method of claim 1, wherein said etch chemistry further includes a fluorocarbon.

16. The method of claim 15, wherein said low capacitance dielectric layer is made of a

silicon-containing low dielectric material.

17. A method for etching a low capacitance dielectric layer in a plasma processing chamber, said low capacitance dielectric layer being disposed below a hard mask layer on a substrate, said method comprising:

etching said hard mask layer to form openings in said hard mark layer;

flowing an etch chemistry that includes O_2 and a hydrocarbon into said plasma processing chamber;

creating a plasma out of said etch chemistry; and

etching, using said plasma, through said low capacitance dielectric layer through said openings in said hard mask layer, said etch chemistry passivating sidewalls of said openings during said etching of said low capacitance dielectric layer to allow substantially vertical profiles.

18. The method of claim 17, wherein said etch chemistry further includes N_2.

19. The method in claim 17, wherein etching said hard mask layer and etching said low capacitance dielectric layer are performed in a single processing chamber.

20. A method for etching a low capacitance dielectric layer in a plasma processing chamber, said low capacitance dielectric layer being disposed below a hard mask layer on a substrate, said hard mask disposed below a photoresist mask, said method comprising:

patterning an opening in said photoresist mask;

patterning said hard mask layer using said opening in said photoresist mask;

flowing an etch chemistry that includes N_2, O_2 , and a hydrocarbon into said plasma processing chamber;

creating a plasma out of said etch chemistry; and

etching, using said plasma, through said low capacitance dielectric layer through said openings in said hard mask layer.

21. The method of claim 20, wherein said photoresist mask is removed during etching.

22. The method of claim 20, wherein said etch chemistry further includes a fluorocarbon.

23. The method of claim 20, wherein said hydrocarbon is one of C_2H_4 and CH_4.

24. The method of claim 20, wherein said photoresist mask is removed prior to etching.

25. The method of claim 20, wherein said plasma processing chamber represents one of an inductively coupled plasma processing chamber and a capacitive-type plasma processing chamber.

26. The method of claim 20, wherein said hydrocarbon and said O_2 are present in the etch chemistry at a ratio of between about 2:1 and about 1:99.

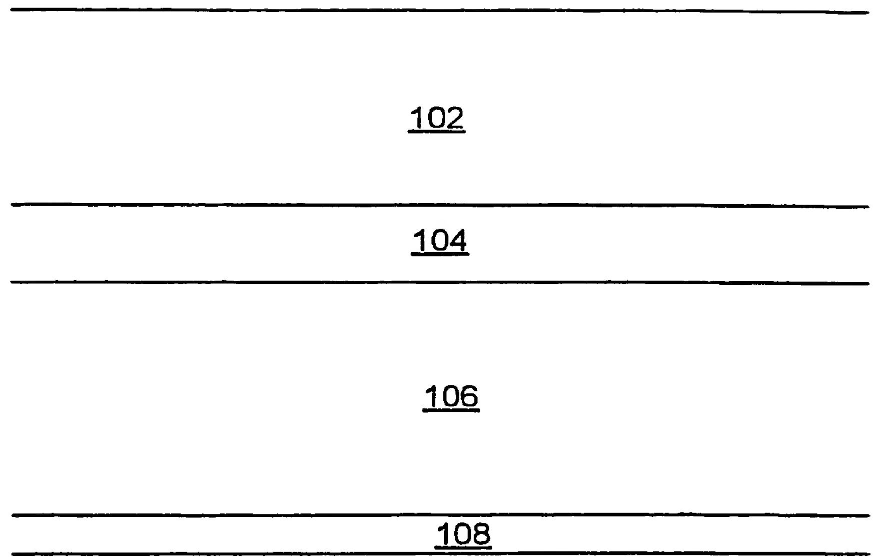


Fig. 1

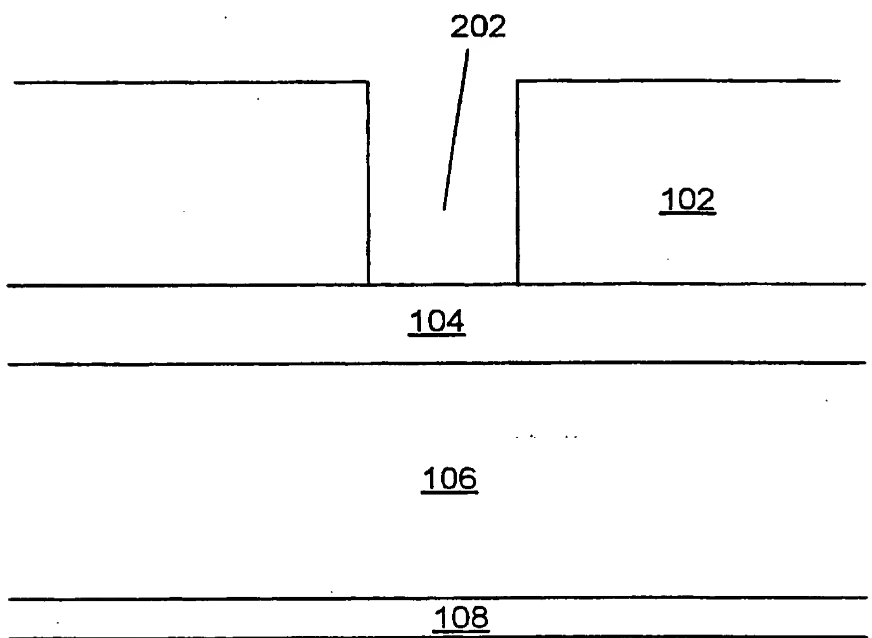
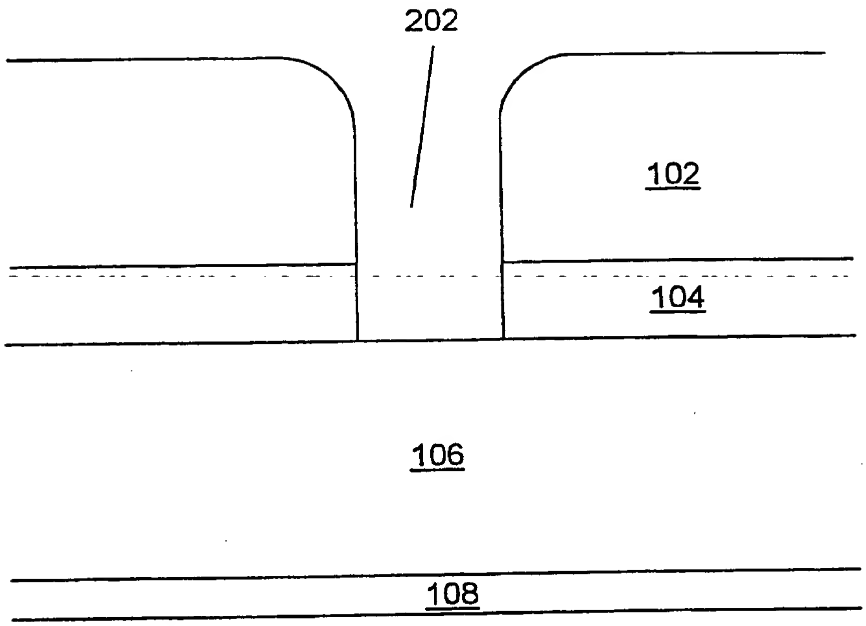


Fig. 2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104
106
108

Fig. 3

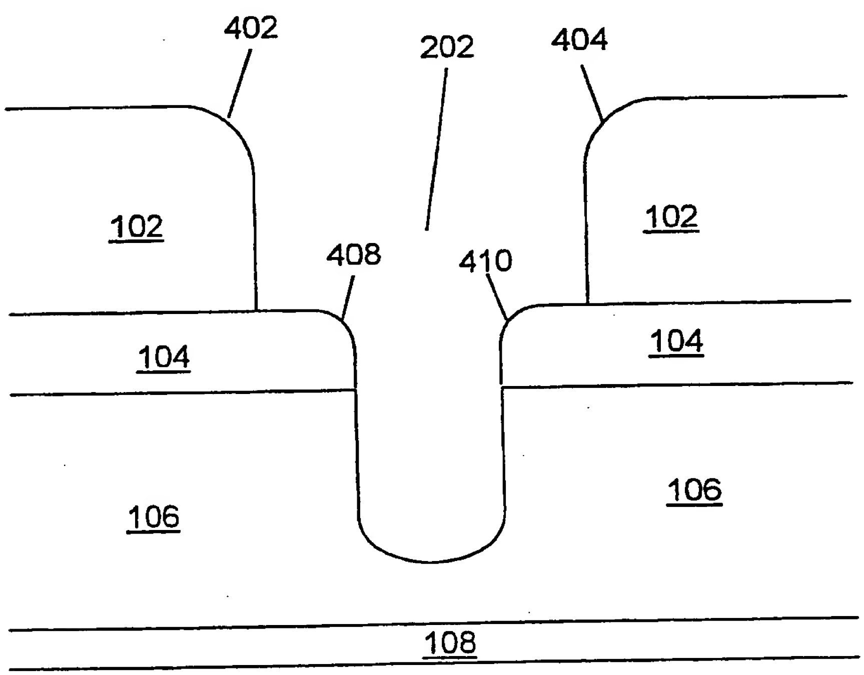
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Fig. 4

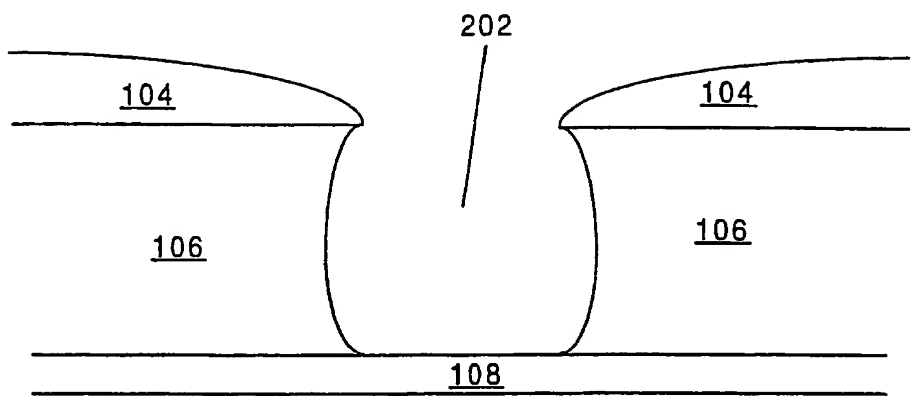


Fig. 5

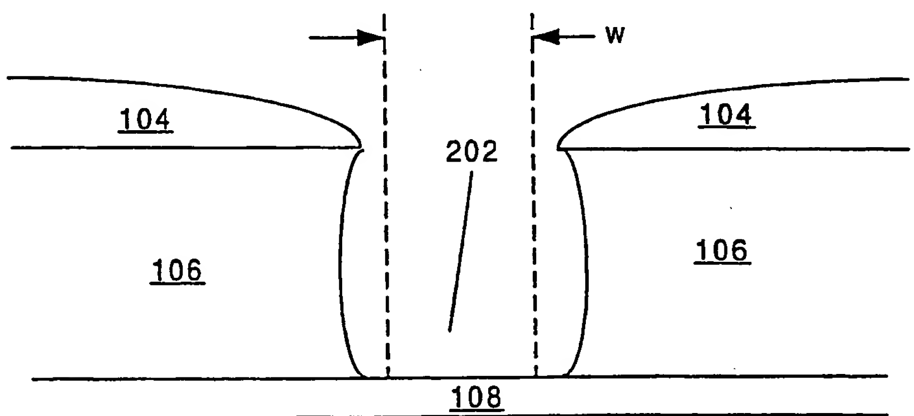


Fig. 6

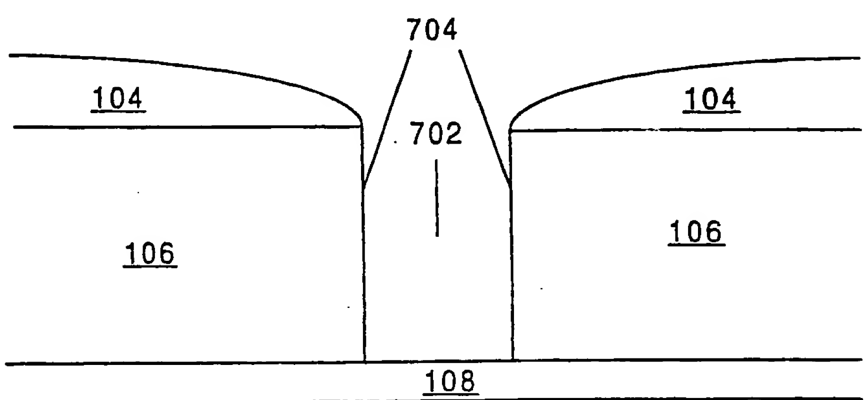
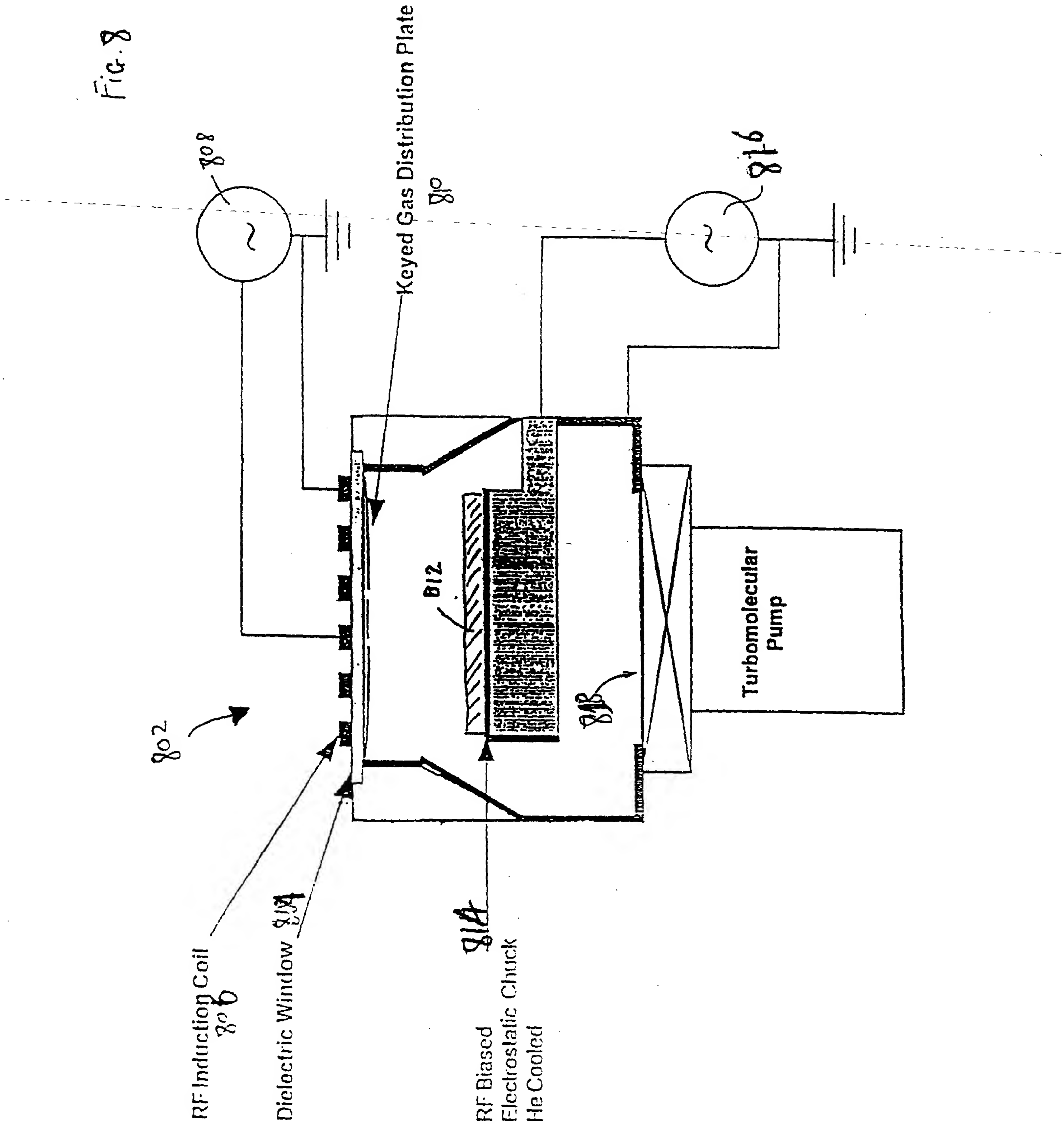


Fig. 7

Fig. 8


802
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816
812
818
Turbomolecular Pump
RF Induction Coil
806
Dielectric Window
804
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RF Biased
Electrostatic Chuck
He Cooled

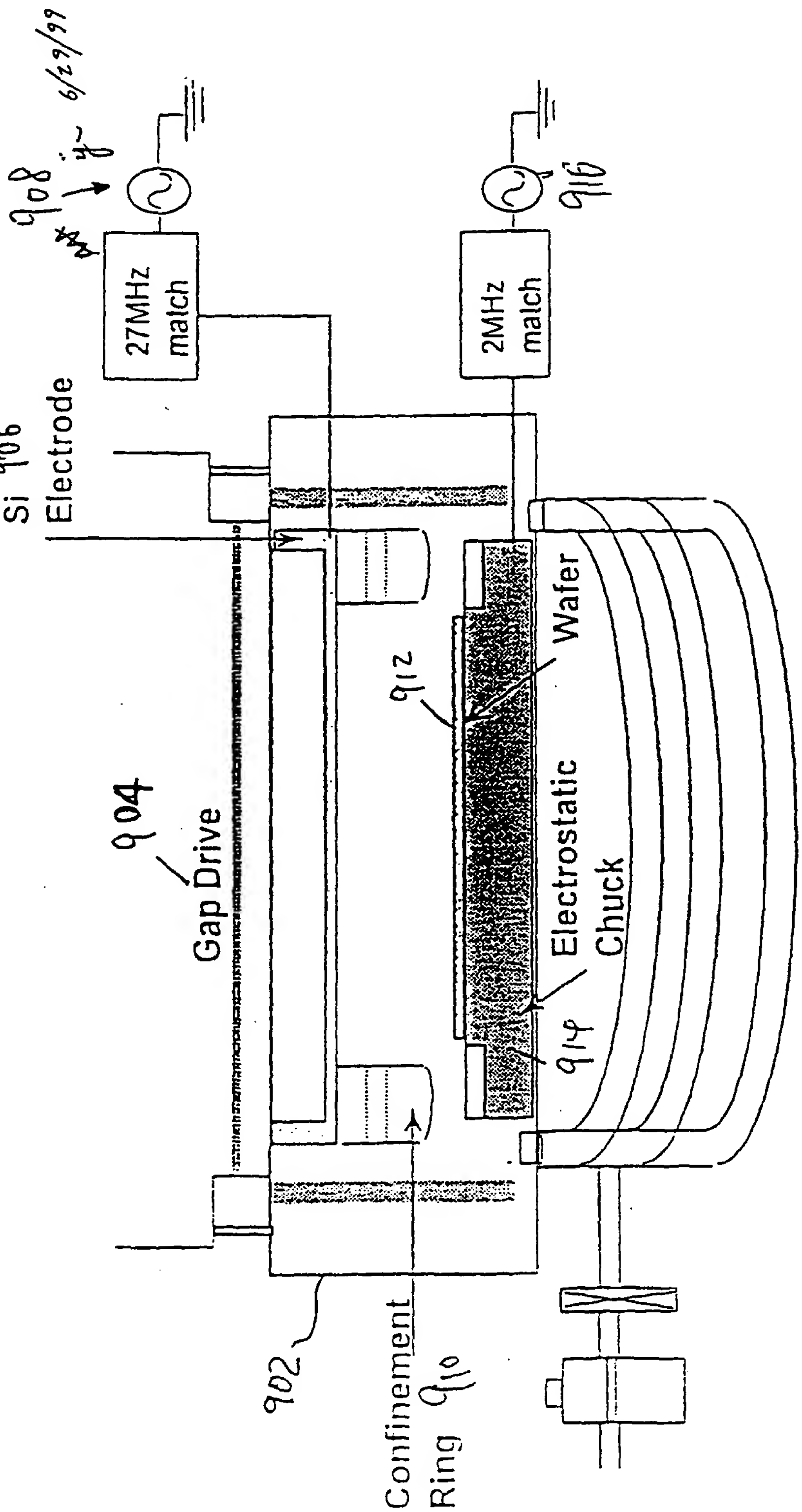
Si 906
Electrode
27MHz match
908
6/29/99
2MHz match
916
904
Gap Drive
912
Wafer
Electrostatic Chuck
914
902
Confinement Ring 910

Fig. 9

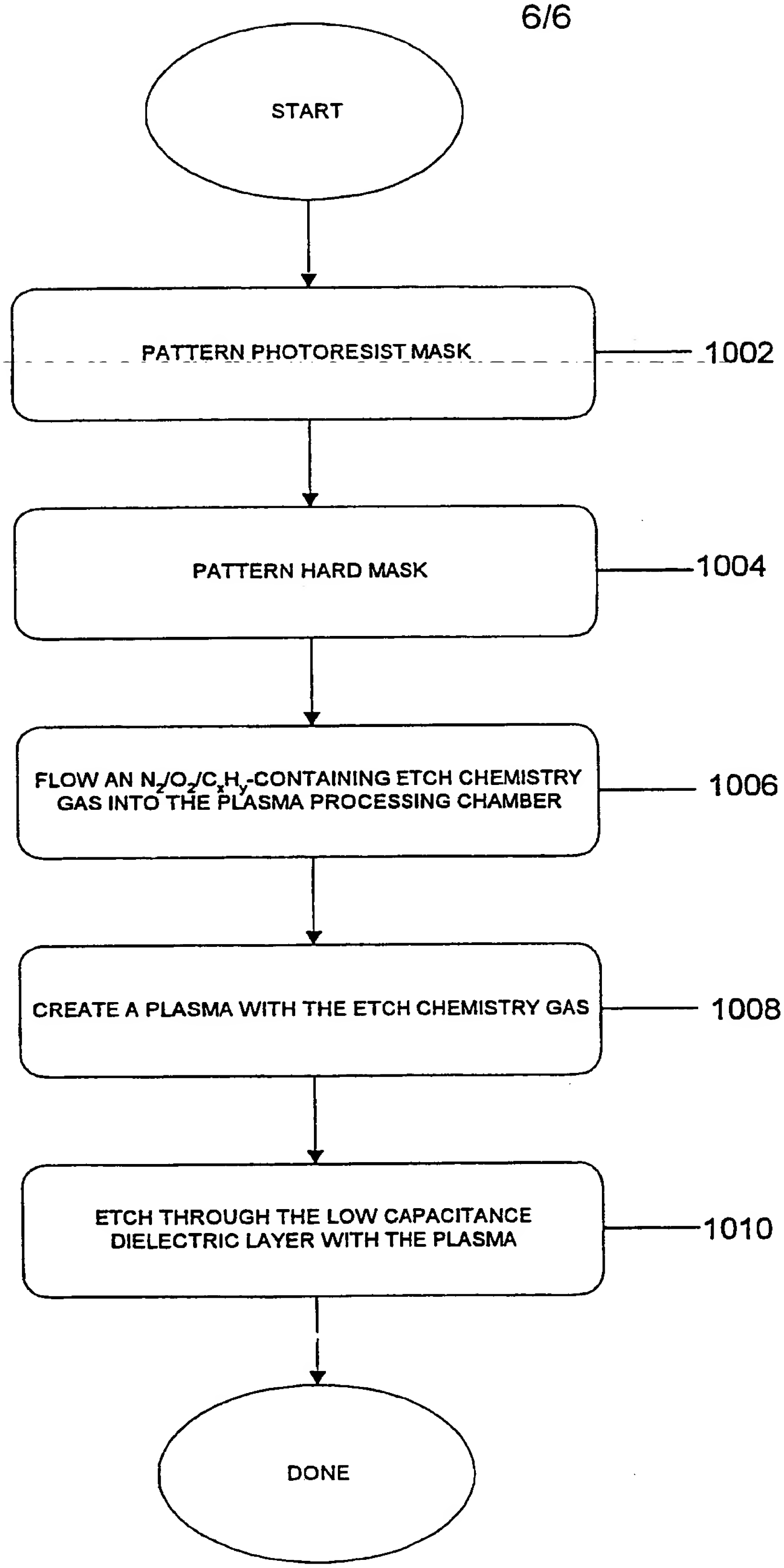
START
PATTERN PHOTORESIST MASK
1002
PATTERN HARD MASK
1004
FLOW AN $N_2/O_2/C_xH_y$-CONTAINING ETCH CHEMISTRY GAS INTO THE PLASMA PROCESSING CHAMBER
1006
CREATE A PLASMA WITH THE ETCH CHEMISTRY GAS
1008
ETCH THROUGH THE LOW CAPACITANCE DIELECTRIC LAYER WITH THE PLASMA
1010
DONE

Fig. 10

INTERNATIONAL SEARCH REPORT

Inte   ional Application No
PCT/US 00/12356

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/311

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

PAJ, EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 268 (E-775), 20 June 1989 (1989-06-20) -& JP 01 059820 A (TOKUDA SEISAKUSHO LTD), 7 March 1989 (1989-03-07)	1,2,10, 15,20, 22,23
Y	abstract	1,20
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 213 (E-759), 18 May 1989 (1989-05-18) -& JP 01 025419 A (MATSUSHITA ELECTRIC IND CO LTD), 27 January 1989 (1989-01-27)	17,19
Y	abstract	1,20

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
8 September 2000	18/09/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Gori, P

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Inte[r]national Application No
PCT/US 00/12356

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	SHUZO FUJIMURA ET AL: "ADDITIVE NITROGEN EFFECTS ON OXYGEN PLASMA DOWNSTREAM ASHING" JAPANESE JOURNAL OF APPLIED PHYSICS,JP,PUBLICATION OFFICE JAPANESE JOURNAL OF APPLIED PHYSICS. TOKYO, vol. 29, no. 10, 1 October 1990 (1990-10-01), pages 2165-2170, XP000224008 ISSN: 0021-4922 abstract	1,20
A	WO 96 19826 A (THOMAS) 27 June 1996 (1996-06-27) abstract	1,17,20

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INTERNATIONAL SEARCH REPORT

.nformation on patent family members

Inte ional Application No
PCT/US 00/12356

Patent document cit d in search report	Publication dat	Patent family member(s)	Publication date
JP 01059820 A	07-03-1989	NONE	
JP 01025419 A	27-01-1989	NONE	
WO 9619826 A	27-06-1996	NONE	